USING THE ASYCHRONOUS COMMUNICATION ADAPTER WITH THE MOTOROLA 68HC11 PROCESSOR FAMILY

The ASYCHRONOUS (ASYNC) COMMUNICATION ADAPTER provides the EPROM+ system with a complete asychronous communication subsystem. This subsystem allows the EPROM+ to support the Motorola 68HC11 family of microcontrollers via the on-chip serial communication interface in conjunction with the processors “BOOTSTRAP” mode.

INSTALLING THE ADAPTER INTO THE PROGRAMMING UNIT

To install the adapter into the programming unit, lift the handle on the 32 pin ZIF socket to about 45 degrees. With the adapter fully left justified, insert the pins into the released socket mechanism. Note that the adapter has a 28 pin base and must be fully left justified in the 32 pin socket for proper operation. Release the handle to lock the adapter in place. Connect the adapter pin marked “+5” to the “+5” pin on the programming unit ACCESSORY CONNECTOR. The adapter is now ready for use.

ABOUT THE 68HC11 “BOOTSTRAP” MODE

All members of the Motorola 68HC11 family of microcontroller include a special mode of chip operation called “BOOTSTRAP” mode. BOOTSTRAP mode allows any program to be uploaded, using the 68HC11 serial communication interface, into the internal RAM memory of the 68HC11 and then executed. The EPROM+ system uses BOOTSTRAP mode to initially upload a communication program into the 68HC11. The communication program then establishes a link with the EPROM+ system whereby the internal EPROM, EEPROM and I/O become accessable. The 68HC11 processor must be forced to enter “BOOTSTRAP” mode after a processor reset or the initial application of power. Specific conditions must exist for the processor to enter BOOTSTRAP mode. These are:

1. The processor MODE pins (MODA and MODB) must both be at logic 0 or ground when the processor leaves reset or power is applied.

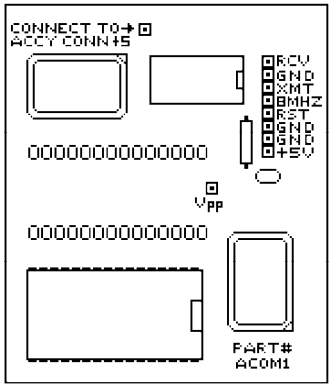
2. The processor must be operating at 8 MHZ. This may be from an externally attached crystal or a supplied frequency source attached to the processor EXTAL pin.

3. The RxD and TxD pins must be unencumbered by circuitry and and be free to attach to the proper pins on the ASYNC adapter.

NOTE: If any of the initial conditions listed above are not valid when the 68HC11 processor leaves reset, the processor will not enter BOOTSTRAP mode and the communication program cannot be uploaded.

CONNECTING THE ASYNC ADAPTER TO THE 68HC11 TARGET PROCESSOR

The ASYNC adapter includes all necessary circuitry to communicate with a 68HC11 processor. Each pin on the adapter is described regarding its connection to the target processor. Read the descriptions below and connect the proper adapter pins to the correct pins on the 68HC11 target processor. Note that no processor pin numbers are referenced as the actual physical target processor package must be used to determine the true pin number. This information may be obtained by examining the processor data sheet.



GND - These pins are connected to the EPROM+ system ground and at least one must be connected to the 68HC11 ground or Vss pin. There are three pins provided if it is necessary to force the MODA or MODB processor pins to 0.

RCV - This is the input to the serial data RECEIVER on the ASYNC adapter. It must be connected to the TxD (transmit) pin on the processor.

XMT - This is the output from the serial data TRANSMITTER on the ASYNC adapter. It must be connected to the RxD (receive) pin on the processor.

8MZ - This is an 8 MHZ source which may be connected to the processor EXTAL pin if needed.

RST - This pin is available to manually reset the processor before the BOOTSTRAP upload begins. It may be connected to the processor RESET line if necessary. It is not necessary to connect this pin if the processor is started from a “power off” state as the “power on” sequence will automatically perform a processor reset.

+5 - This pin is a source of 5 volt power. It may be used to power the processor in “stand-alone” operation but should not be used to power a complete circuit assembly. Current capacity is approximately 100mA.

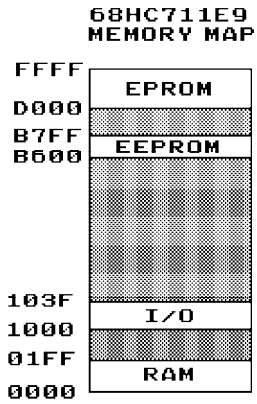
Vpp - This separate pin supplies the high voltage (12.75V) which is required to program the internal EPROM in 68HC11 processors which contain EPROM. This pin is not connected for reading or programming the internal EEPROM or configuration register. This pin is attached to the Vpp pin on the processor. **Warning:** Do not connect this pin unless you are absolutely certain that external circuitry connected to the processor XIRQ/Vpp pin will not be damaged.

INITIATING COMMUNICATIONS WITH THE TARGET PROCESSOR

Before initiating communications with the target 68HC11 processor, the processor must have power applied and have successfully entered “BOOTSTRAP” mode from reset. If you have connected the adapter RST pin to the processor RESET pin, the EPROM+ software will automatically generate a processor reset before performing the program upload. The communicaton program upload is initiated using the “Z” command (DEVICE OPTIONS). Press “Z”. You will see three options. Press “1”. This will automatically read the communication program into the system buffer and perform the upload operation. You will see the following messages: “BOOTSTRAP UPLOAD IN PROGRESS...”, “BUFFER UPLOAD COMPLETE”, “COMMUNICATION VERIFIED”. The system indicates the current operation. The last message (COMMUNICATION VERIFIED) must be displayed in order for the EPROM+ to communicate with the target processor. If this message is not displayed, the communication program is not active and the target processor may not be accessed. If the “COMMUNICATION VERIFIED” message is not displayed, verify that the conditions listed under “CONNECTING THE ASYNC ADAPTER TO THE 68HC11 TARGET PROCESSOR” are correct. NOTE: If you have not connected the adapter RST pin to the target processor the system will display: “WARNING! CONNECTION NOT CONFIRMED FROM TARGET PROCESSOR AFTER RESET”. This message indicates that the EPROM+ system did not receive a confirmation from the target processor after the EPROM+ system initiated a reset. This is a normal message if you do not have the RST pin connected. After the processor is reset in “BOOTSTRAP” mode, it transmits a single response called a “BREAK”. The EPROM+ software checks for the “BREAK” response after the reset. If you manually reset the processor by applying power, the “BREAK” response occurs before the EPROM+ is ready. This in no way causes a problem and the program upload progresses normally.

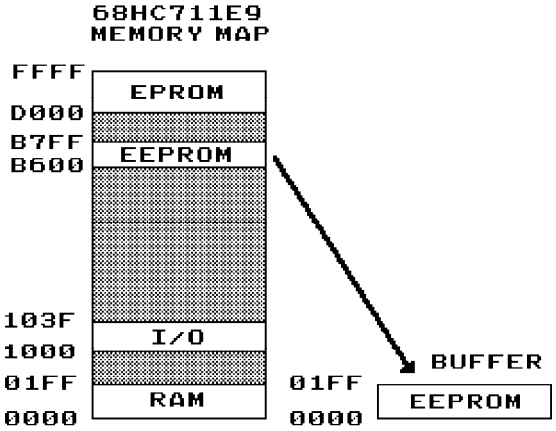
ACCESSING THE INTERNAL MEMORY OF THE 68HC11

Once communication has been established with the target processor, all EPROM+ software functions are available to access the internal memory of the 68HC11. The EPROM+ software remains in communication with the target processor until you exit the program, change the device type or power down the target. The internal memory of the 68HC11 depends on the series of part with which you are working. For purposes of illustration, this example will use the 68HC711E9. The 68HC711E9 actually has three accessable areas of memory. These are RAM, EEPROM and EPROM (see first figure). While the communication program is active it occupies the lower 256 bytes of RAM (0-FF). Note that the EEPROM exists between addresses B600 and B7FF (512 bytes) and EPROM exists between D000 and FFFF (12K bytes). The EPROM+ sofware allows you to easily work with the EEPROM or EPROM as if it were the only memory in the part. This means, for example, that you may work with the EEPROM as if it were an individual memory part of 512 bytes with a starting address of 0 and an ending address of 1FF (see second figure). This is much easier than working with the memory map offset of B600 to B7FF. The same is true for the EPROM. The software automatically remaps the EEPROM such that if you read the part, the EEPROM data will appear in the buffer from 0 to 1FF. The system defaults to EEPROM for the area of the memory map which will be accessed if the part contains EEPROM. If the part only contains EPROM or RAM, the system will default to EPROM first, then RAM.



CHANGING THE AREA OF ACCESS

The software allows you to change the memory area accessed by the system. This is accomplished from the “O”ptions selection from the first set of “UPLOAD (BOOTSTRAP) PROGRAM TO DEVICE” options. Press “O”. You are presented with three memory access areas. Choose the area you wish to remap to buffer address 0. Note: These options are always displayed even if the part does not have the memory physically implemented. If you attempt to access EEPROM in a part within which the memory does not exist, you will be notified with an error message. Once the desired area is selected, the software automatically uses the proper programming algorithm. The current area will remain active until it is changed or the system is shut down.



FEATURES FOR ADVANCED USERS

The standard access provided for EEPROM/EPROM reading and programing are more than adequate for typical maintenance and service applications. The software, however, has features for the technically advanced user who has interest in product development or testing of existing systems. The following features are provided:

1. Upload (bootstrap) any program you wish from the system buffer into the 68HC11.
2. Access the entire 64K address range of the processor including all memory and I/O registers.
3. Select the programming algorithm to be used while accessing the 64K range.
4. Transfer control to a "USER PROGRAM" and display a returned "BYTE" value.

Each feature is described below.

1. Upload (bootstrap) any program into the 68HC11

This feature is accessed from the initial "Z" (DEVICE OPTIONS) option list. In addition to Option 1, which uploads the communication program into the 68HC11, Option 2 will upload the first 256 bytes of the system buffer into the processor and then transfer control to the program at address 0. Option 3 performs the same function except you have the option of specifying the exact number of bytes to upload. This value may be from 0 to FFFF. You will be prompted for the buffer ending address at which the upload will cease.

2. Access the entire 64K address range

This feature is accessed from the same option selections used to choose the memory access area. Choose Option 3 (ENTIRE 64K ADDRESS RANGE). This causes the buffer addresses to exactly match the device addresses. For example if you perform a ZONE READ (Command 3 - Option 2) at device address B600 through B7FF into the buffer at address B600 you will read the internal EEPROM of a 68HC711E9 and place the information into the buffer at exactly the same addresses at which it exists in the processor. This access mode allows you to view and modify any location you choose within the processor. Use caution as this access mode also allows you access to the first 256 (0-FF) bytes of RAM where the communications program resides.

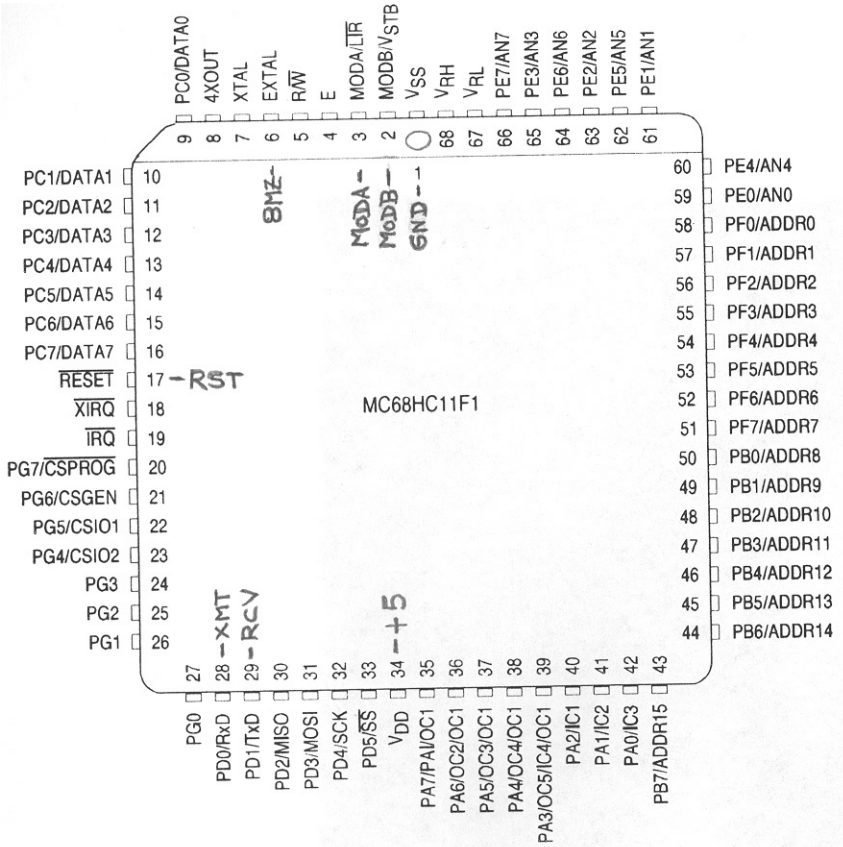
3. Select the programming algorithm to be used while accessing the 64K range

This feature is accessed as an option under "MEMORY ACCESS OPTIONS". Note that the 64K range must be selected as the current access option before the programming algorithm may be changed. Once the "PROGRAMMING ALGORITHM FOR 64K RANGE" is displayed, choose the algorithm which is to be used by the system for programming. With the selections available, you may perform direct RAM and I/O writes, EEPROM writes or EPROM writes. Note that Vpp (12.75V) must be applied to the processor Vpp pin before the internal EPROM may be programmed. You may use this feature to change the setting of the CONFIGURATION register which is implemented with EEPROM cells.

4. Transfer control to a "USER PROGRAM" and display a returned "BYTE" value

This feature is accessed as an option under "PROGRAMMING ALGORITHM FOR 64K RANGE". It is specifically intended for the testing of small user programs loaded into RAM, EEPROM or EPROM. The program to be executed (user program) must be loaded into the processors physical memory. This may be accomplished using the buffer "WRITE" command which writes a block of data from anywhere in the buffer to anywhere in the device. Once the program in transferred to the 68HC11 memory, enter the starting address for the program at the prompt and press <ENTER>. Control will be transferred to the program at the specified address. The EPROM+ software will now wait for a byte to be returned from the user program. If you wish to view a returned byte from the user program it must be loaded into Accumulator A (ACCA) of the 68HC11. A "JUMP TO SUBROUTINE" (JSR) must then be executed to fixed address $0005. This will cause the byte in ACCA to be transmitted via the communication program back to the EPROM+ software where it is displayed to the operator. This "RETURN BYTE" capability allows you to monitor data or status from your program which may be used for testing or debugging. Note that ACCA is destroyed by the transmit subroutine. To return control to the EPROM+ software from the user program you may execute an extended (16 bit) jump (JMP) to address $0008. This will allow you to again access the 64K address range after your program is done executing. This is useful if your program has left data or status information in memory that you wish to examine. Note: You may terminate the "RETURN BYTE" monitoring loop of the EPROM+ software while the user program is executing by pressing ESC.

NOTES: The stack is located at address $00FF. There are about 8 bytes of free stack space after the communication program. If your program requires more space then the stacked should be moved. The communication program occupies the first 256 bytes including the stack. If you overwrite this area communications will be lost and the communication program will need to be reloaded. The communication program uses the 68HC11 SCI.


MC68HC11F1
PC0/DATA0
4XOUT
XTAL
EXTAL
R/W
E
MODA/LIR
MODB/VSTB
VSS
VRH
VRL
PE7/AN7
PE3/AN3
PE6/AN6
PE2/AN2
PE5/AN5
PE1/AN1
PC1/DATA1
PC2/DATA2
PC3/DATA3
PC4/DATA4
PC5/DATA5
PC6/DATA6
PC7/DATA7
RESET
XIRQ
IRQ
PG7/CSPROG
PG6/CSGEN
PG5/CSIO1
PG4/CSIO2
PG3
PG2
PG1
PE4/AN4
PE0/AN0
PF0/ADDR0
PF1/ADDR1
PF2/ADDR2
PF3/ADDR3
PF4/ADDR4
PF5/ADDR5
PF6/ADDR6
PF7/ADDR7
PB0/ADDR8
PB1/ADDR9
PB2/ADDR10
PB3/ADDR11
PB4/ADDR12
PB5/ADDR13
PB6/ADDR14
PG0
PD0/RxD
PD1/TxD
PD2/MISO
PD3/MOSI
PD4/SCK
PD5/SS
VDD
PA7/PAI/OC1
PA6/OC2/OC1
PA5/OC3/OC1
PA4/OC4/OC1
PA3/OC5/IC4/OC1
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PA0/IC3
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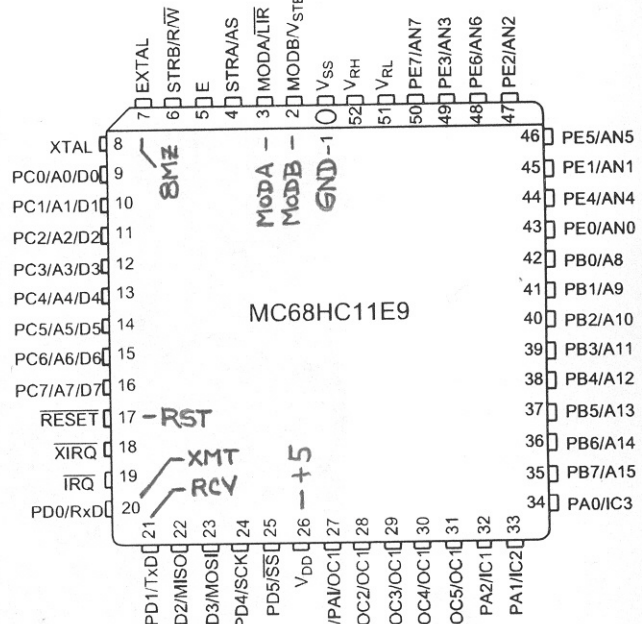
BMZ
MODA
MODB
GND
RST
XMT
RCV
+5


MC68HC11E9
EXTAL
STRB/R/W
E
STRA/AS
MODA/LIR
MODB/VSTBY
VSS
VRH
VRL
PE7/AN7
PE3/AN3
PE6/AN6
PE2/AN2
XTAL
PC0/A0/D0
PC1/A1/D1
PC2/A2/D2
PC3/A3/D3
PC4/A4/D4
PC5/A5/D5
PC6/A6/D6
PC7/A7/D7
RESET
XIRQ
IRQ
PD0/RxD
PE5/AN5
PE1/AN1
PE4/AN4
PE0/AN0
PB0/A8
PB1/A9
PB2/A10
PB3/A11
PB4/A12
PB5/A13
PB6/A14
PB7/A15
PA0/IC3
PD1/TxD
PD2/MISO
PD3/MOSI
PD4/SCK
PD5/SS
VDD
PA7/PAI/OC1
PA6/OC2/OC1
PA5/OC3/OC1
PA4/OC4/OC1
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PA2/IC1
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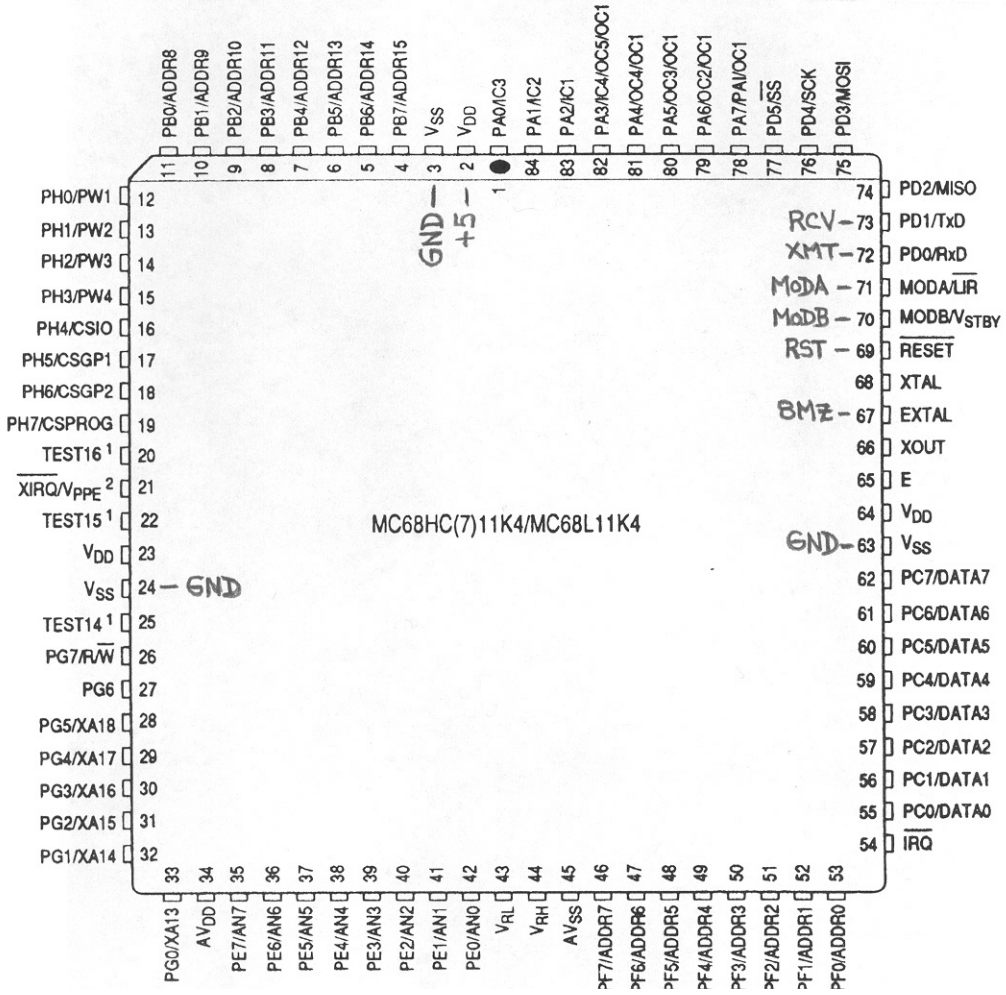
BMZ
MODA
MODB
GND
RST
XMT
RCV
+5


MC68HC(7)11K4/MC68L11K4
PB0/ADDR8
PB1/ADDR9
PB2/ADDR10
PB3/ADDR11
PB4/ADDR12
PB5/ADDR13
PB6/ADDR14
PB7/ADDR15
VSS
VDD
PA0/IC3
PA1/IC2
PA2/IC1
PA3/IC4/OC5/OC1
PA4/OC4/OC1
PA5/OC3/OC1
PA6/OC2/OC1
PA7/PAI/OC1
PD5/SS
PD4/SCK
PD3/MOSI
PH0/PW1
PH1/PW2
PH2/PW3
PH3/PW4
PH4/CSIO
PH5/CSGP1
PH6/CSGP2
PH7/CSPROG
TEST16 1
XIRQ/VPPE 2
TEST15 1
VDD
VSS
TEST14 1
PG7/R/W
PG6
PG5/XA18
PG4/XA17
PG3/XA16
PG2/XA15
PG1/XA14
PD2/MISO
PD1/TxD
PD0/RxD
MODA/LIR
MODB/VSTBY
RESET
XTAL
EXTAL
XOUT
E
VDD
VSS
PC7/DATA7
PC6/DATA6
PC5/DATA5
PC4/DATA4
PC3/DATA3
PC2/DATA2
PC1/DATA1
PC0/DATA0
IRQ
PG0/XA13
AVDD
PE7/AN7
PE6/AN6
PE5/AN5
PE4/AN4
PE3/AN3
PE2/AN2
PE1/AN1
PE0/AN0
VRL
VRH
AVSS
PF7/ADDR7
PF6/ADDR6
PF5/ADDR5
PF4/ADDR4
PF3/ADDR3
PF2/ADDR2
PF1/ADDR1
PF0/ADDR0
GND
+5
RCV
XMT
MODA
MODB
RST
BMZ